

AMENDMENT AND RESPONSE

Serial Number: 08/903,486

Filing Date: July 29, 1997

Title: SILICON CARBIDE GATE TRANSISTOR

Page 2

Dkt: 303.326US1

silicon carbide compound $\text{Si}_{1-x}\text{C}_x$, wherein x is less than 0.5, and being connected to receive a second input signal.

Sub
E1
D3

15. [Twice Amended] A semiconductor memory device comprising:
a memory array including a plurality of transistors, at least one of the transistors in a semiconductor surface layer formed on an underlying insulating portion and including an electrically interconnected gate formed of a silicon carbide [material] compound $\text{Si}_{1-x}\text{C}_x$, wherein x is less than 0.5, the gate being connected to receive an input signal;
addressing circuitry [for addressing] to address the memory array; and
control circuitry [for controlling] to control read, write, and erase operations of the memory device.

Sub
E1
D4

24. [Amended] The semiconductor memory device of claim 15 wherein [each] a plurality of the transistors in the memory array [comprises] comprise:
a source region, a drain region, and a channel region between the source and drain regions in a semiconductor surface layer formed on an underlying insulating portion; and
an electrically interconnected gate formed of a silicon carbide [material] compound $\text{Si}_{1-x}\text{C}_x$, wherein x is less than 0.5, the gate being connected to receive an input signal.

Sub
E1
D5

25. [Twice Amended] The semiconductor memory device of claim 15 wherein pairs of the transistors in the memory array comprise:
a substrate;
a p-channel transistor formed in a first portion of the substrate, the p-channel transistor including a source region, a drain region, a channel region between the source and drain regions, and an electrically interconnected silicon carbide gate over the channel region and separated therefrom by an insulating layer, the gate of the p-channel transistor comprising a silicon carbide compound $\text{Si}_{1-x}\text{C}_x$, wherein x is less than 0.5, and being connected to receive a first input signal;
and
an n-channel transistor formed in a second portion of the substrate, the n-channel transistor including a source region, a drain region, a channel region between the source and

AMENDMENT AND RESPONSE

Serial Number: 08/903,486

Filing Date: July 29, 1997

Title: SILICON CARBIDE GATE TRANSISTOR

Page 3

Dkt: 303.326US1

DS
Cont

drain regions, and an electrically interconnected silicon carbide gate over the channel region and separated therefrom by an insulating layer, the gate of the n-channel transistor comprising a silicon carbide compound $\text{Si}_{1-x}\text{C}_x$, wherein x is less than 0.5, and being connected to receive a second input signal.

Sub
D6

27. [Twice Amended] The semiconductor memory device of claim 15 wherein the silicon carbide [material] compound $\text{Si}_{1-x}\text{C}_x$ comprises polycrystalline silicon carbide.

28. [Twice Amended] The semiconductor memory device of claim 15 wherein the silicon carbide [material] compound $\text{Si}_{1-x}\text{C}_x$ comprises microcrystalline silicon carbide.

Sub
D7

31. [Twice Amended] A semiconductor memory device comprising:
a memory array including a plurality of transistors wherein pairs of the transistors comprise:

- a substrate;
- a p-channel transistor formed in a first portion of the substrate, the p-channel transistor including a source region, a drain region, a channel region between the source and drain regions, and an electrically interconnected silicon carbide gate over the channel region and separated therefrom by an insulating layer, the gate of the p-channel transistor comprising a silicon carbide compound $\text{Si}_{1-x}\text{C}_x$, wherein x is less than 0.5, and being connected to receive a first input signal; and
- an n-channel transistor formed in a second portion of the substrate, the n-channel transistor including a source region, a drain region, a channel region between the source and drain regions, and an electrically interconnected silicon carbide gate over the channel region and separated therefrom by an insulating layer, the gate of the n-channel transistor comprising a silicon carbide compound $\text{Si}_{1-x}\text{C}_x$, wherein x is less than 0.5, and being connected to receive a second input signal;

addressing circuitry to address the memory array; and
control circuitry to control read, write, and erase operations of the memory device.

Sub
E1
D8

37. [Amended] A transistor comprising:

a substrate having a source region, a drain region, and a channel region between the source region and the drain region formed in the substrate;

an insulating layer on the substrate over the channel region; and

a gate comprising a p+ doped silicon carbide compound $[\text{SiC}] \text{Si}_{1-x}\text{C}_x$ on the insulating layer, wherein x is less than 0.5, the gate being electrically interconnected to receive an input signal.

38. [Amended] The transistor of claim 37 wherein:

the substrate comprises a silicon surface layer formed on an underlying insulating portion having a source region, a drain region, and a channel region between the source region and the drain region formed in the silicon surface layer;

the insulating layer comprises gate oxide or tunnel oxide;

the silicon carbide compound $[\text{SiC}] \text{Si}_{1-x}\text{C}_x$ comprises polycrystalline silicon carbide or microcrystalline silicon carbide, or both polycrystalline and microcrystalline silicon carbide; and

the silicon carbide compound $[\text{SiC}] \text{Si}_{1-x}\text{C}_x$ is p+ doped with boron.

Sub
E1
D9

41. [Amended] A transistor comprising:

a substrate having a source region, a drain region, and a channel region between the source region and the drain region formed in the substrate;

an insulating layer on the substrate over the channel region; and

a gate comprising an n+ doped silicon carbide compound $[\text{SiC}] \text{Si}_{1-x}\text{C}_x$ on the insulating layer, wherein x is less than 0.5, the gate being electrically interconnected to receive an input signal.

42. [Amended] The transistor of claim 41 wherein:

the substrate comprises a silicon surface layer formed on an underlying insulating portion having a source region, a drain region, and a channel region between the source region and the drain region formed in the silicon surface layer;

the insulating layer comprises gate oxide or tunnel oxide;

AMENDMENT AND RESPONSE

Serial Number: 08/903,486

Filing Date: July 29, 1997

Title: SILICON CARBIDE GATE TRANSISTOR

Page 5

Dkt: 303.326US1

D9
Cons

the silicon carbide compound $[\text{SiC}] \text{Si}_{1-x}\text{C}_x$ comprises polycrystalline silicon carbide or microcrystalline silicon carbide, or both polycrystalline and microcrystalline silicon carbide; and the silicon carbide compound $[\text{SiC}] \text{Si}_{1-x}\text{C}_x$ is n+ doped with phosphorus.

sub
D 10

45. [Amended] A transistor comprising:
a semiconductor surface layer formed on an underlying insulating portion having a source region, a drain region, and a channel region between the source region and the drain region formed in the semiconductor surface layer;
an insulating layer on the semiconductor surface layer over the channel region; and
a gate comprising a silicon carbide compound $[\text{Si}_x\text{C}_{1-x}] \text{Si}_{1-x}\text{C}_x$ on the insulating layer wherein x is less than 0.5, the gate being electrically interconnected to receive an input signal.

46. [Amended] The transistor of claim 45 wherein:
the semiconductor surface layer comprises p-type silicon;
the insulating layer comprises gate oxide or tunnel oxide;
the silicon carbide compound $[\text{Si}_x\text{C}_{1-x}] \text{Si}_{1-x}\text{C}_x$ comprises polycrystalline silicon carbide or microcrystalline silicon carbide, or both polycrystalline and microcrystalline silicon carbide;
the source region comprises n-type silicon; and
the drain region comprises n-type silicon.

sub
D 11

48. [Amended] The transistor of claim 45 wherein the silicon carbide compound $[\text{Si}_x\text{C}_{1-x}] \text{Si}_{1-x}\text{C}_x$ is p+ doped with boron or n+ doped with phosphorus.

D 12
sub

50. [Amended] A transistor comprising:
a semiconductor surface layer formed on an underlying insulating portion having a source region, a drain region, and a channel region between the source region and the drain region formed in the semiconductor surface layer;
an insulating layer on the semiconductor surface layer over the channel region; and
a gate comprising a silicon carbide compound $[\text{Si}_x\text{C}_{1-x}] \text{Si}_{1-x}\text{C}_x$ on the insulating layer wherein x is [greater] less than 0.5, the gate being electrically interconnected to receive an input